

JAPANESE PATENT OFFICE
PATENT JOURNAL
KOKAI PATENT APPLICATION NO. HEI 6[1994]-188362

Technical Disclosure Section

Int. Cl. ⁵ :	H 01 L 25/065 25/07 25/18 H 05 K 1/18 H 01 L 25/08 H 05 K 1/18
Sequence Nos. for Office Use:	H 7128-4E S 7128-4E
Application No.:	Hei 4[1992]-334796
Application Date:	December 16, 1992
Publication Date:	July 8, 1994
No. of Claims:	1 (Total of 5 pages)
Examination Request:	Not requested

PACKING STRUCTURE FOR SEMICONDUCTOR DEVICE

Inventor:	Takeshi Watanabe Fujitsu, Ltd. 1015 Kamiodanaka, Nakahara-ku, Kawasaki- shi, Kanagawa-ken
-----------	---

Applicant:

000005223
Fujitsu, Ltd.
1015 Kamiodanaka,
Nakahara-ku, Kawasaki-
shi, Kanagawa-ken

Agent:

Teiichi Iketa, patent
attorney

[There are no amendments to this patent.]

Abstract

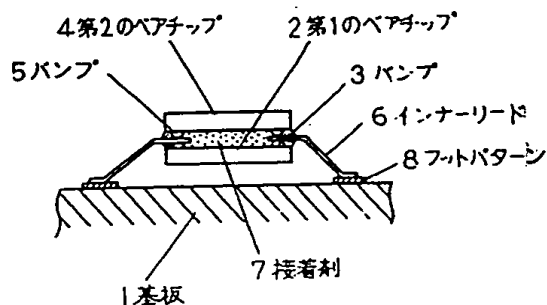
Objective

To provide a packing structure for a semiconductor element, formed to be packed on a substrate by superposing first and second bare chips, and to improve the packing density of the bare chips by being able to pack two bare chips on a prescribed occupied area required for packing one bare chip.

Constitution

First and second bare chips are fixed by superposing, with said mutually fixed first and second bare chips being placed on a prescribed substrate.

Theoretical diagram of this invention



Key: 1 Substrate.
 2 First bare chip
 3 Bump
 4 Second bare chip
 5 Bump
 6 Inner lead
 7 Adhesive
 8 Foot pattern

Claim

A packing structure for a semiconductor characterized by the fact that it is equipped with first and second bare chips (2,4) being superposed so that bumps (3,5) face each other, an inner lead (6) whose one end is sandwiched in each said bump (3,5) and whose other end is fixed to a foot pattern (8) of a substrate (1), with an adhesive (7) being filled between said first and second bare chips (2,4); and characterized in that said first and second bare chips (2,4) are packed on said substrate (1) via said inner lead (6).

* * *